

FIG. 1

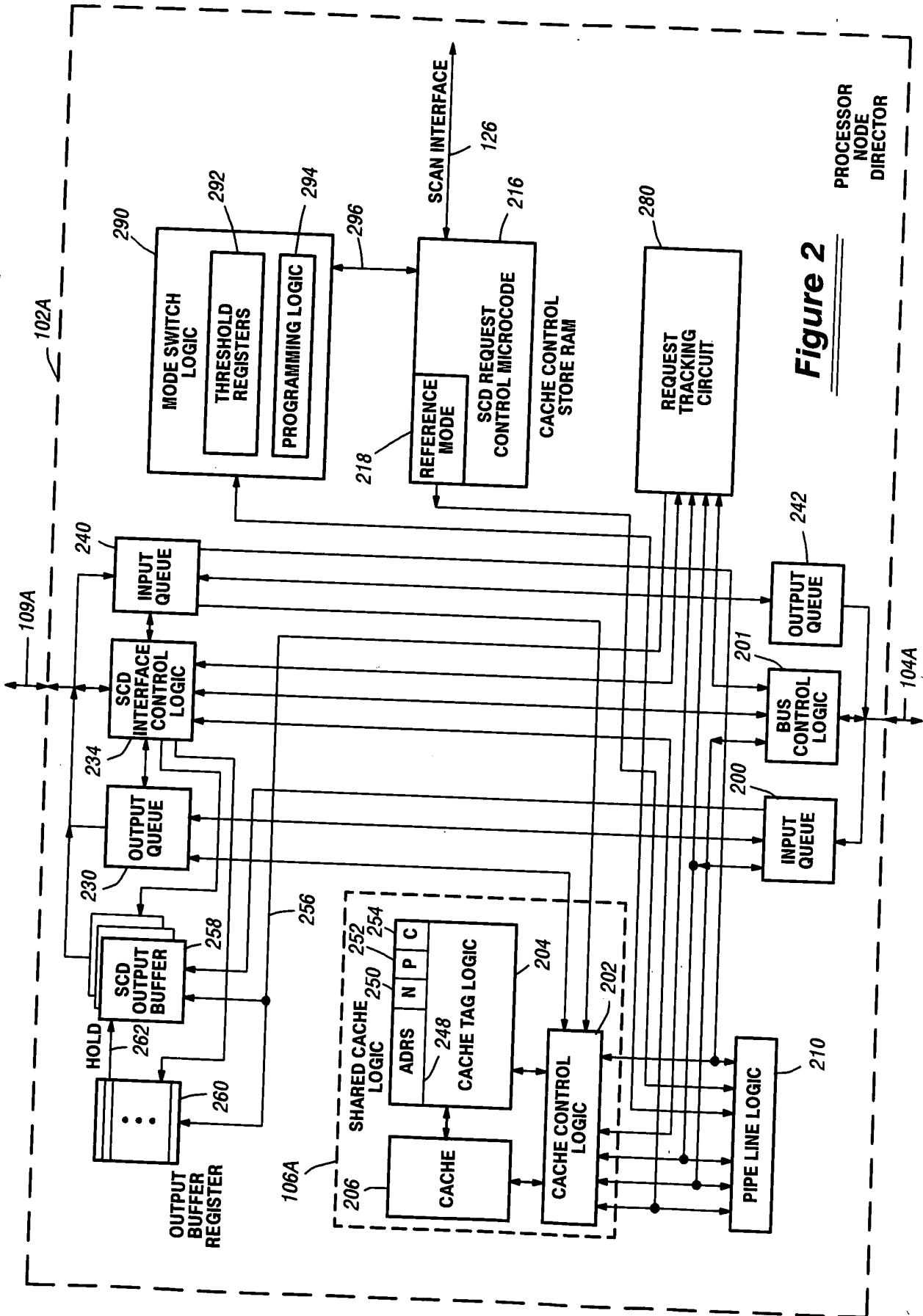


Figure 2

PROCESSOR
NODE
DIRECTOR

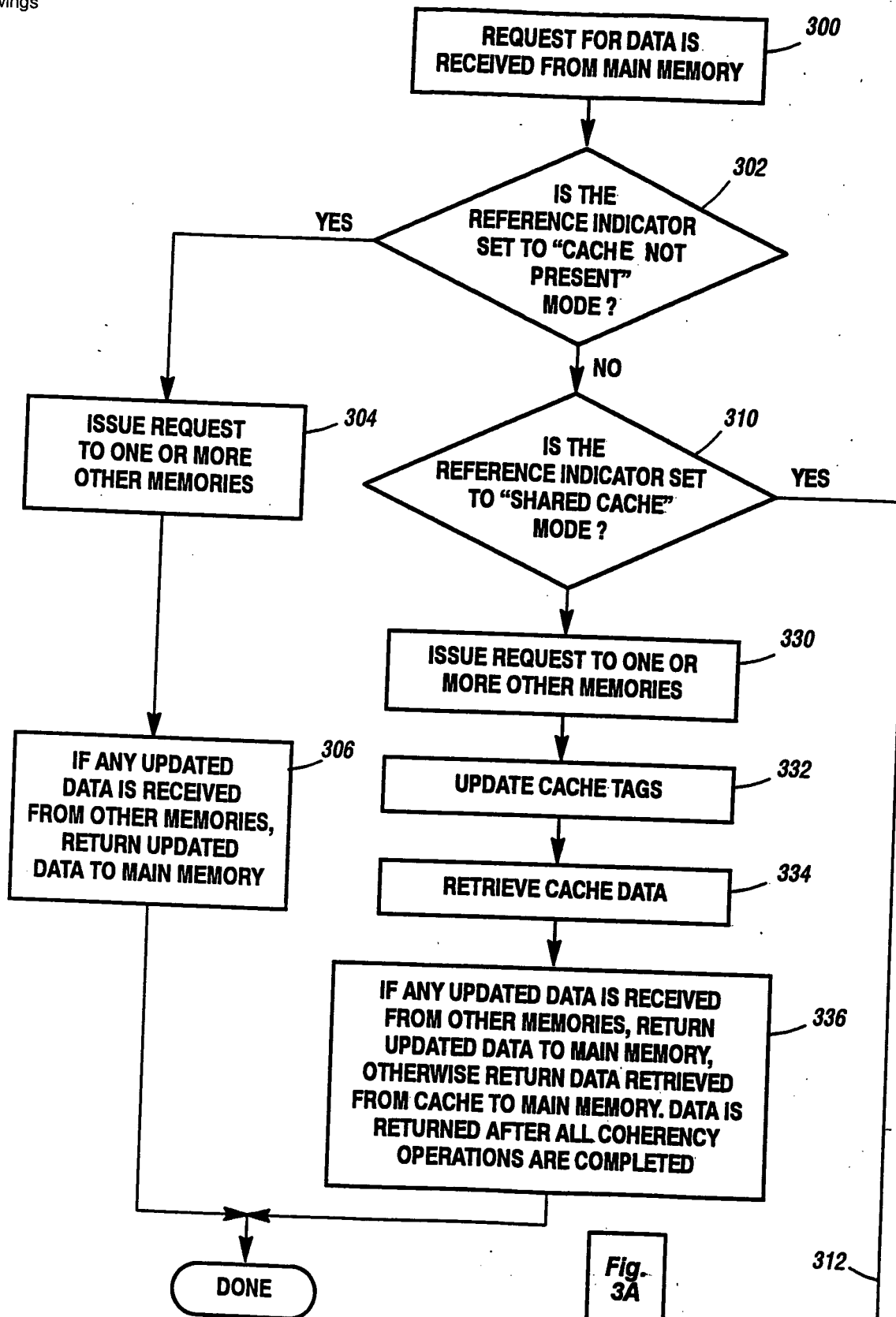


Figure 3A

Fig.
3A

Fig.
3B

Figure 3

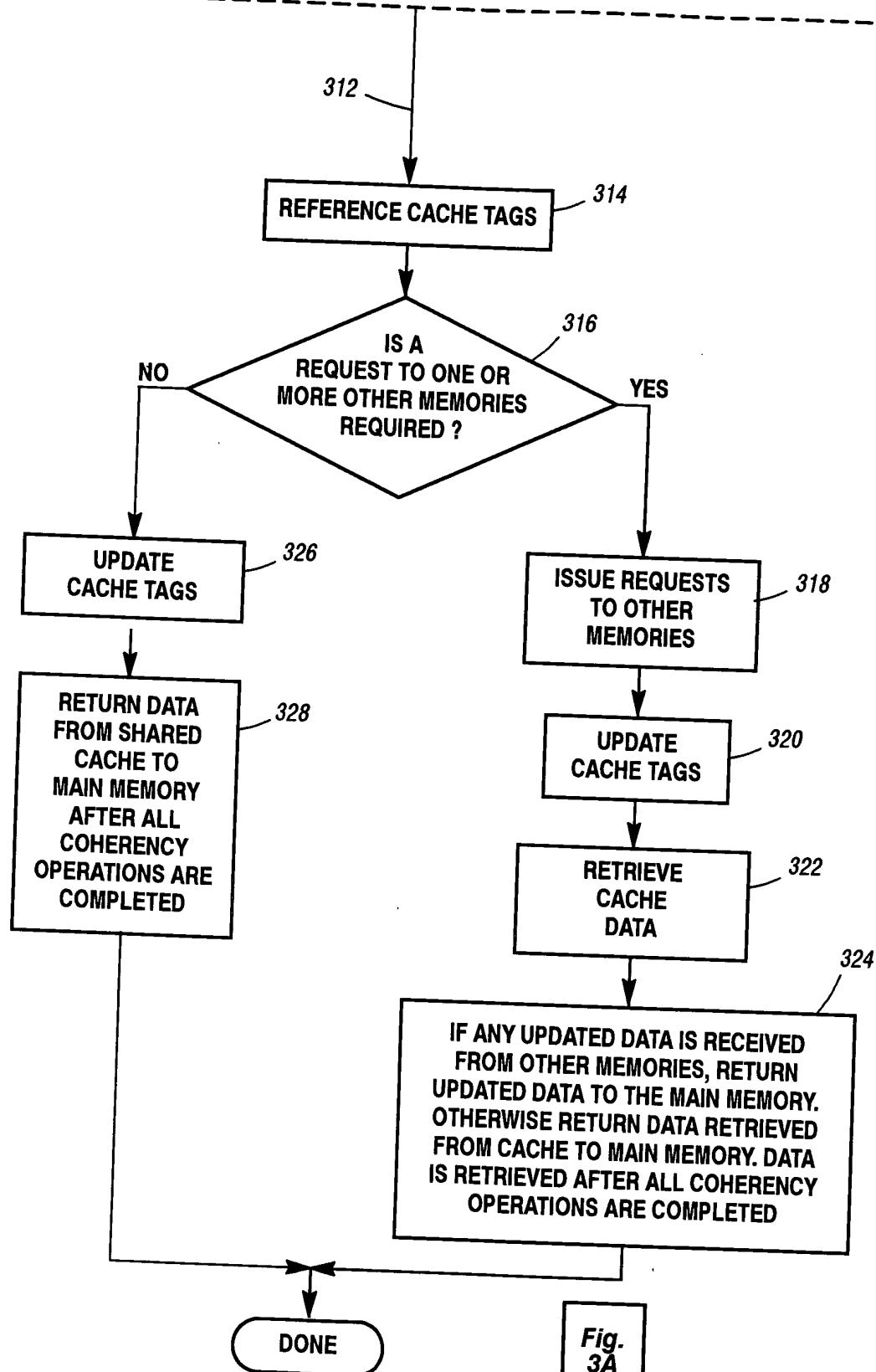


Figure 3B

Fig.
3A

**Fig.
3B**

Figure 3

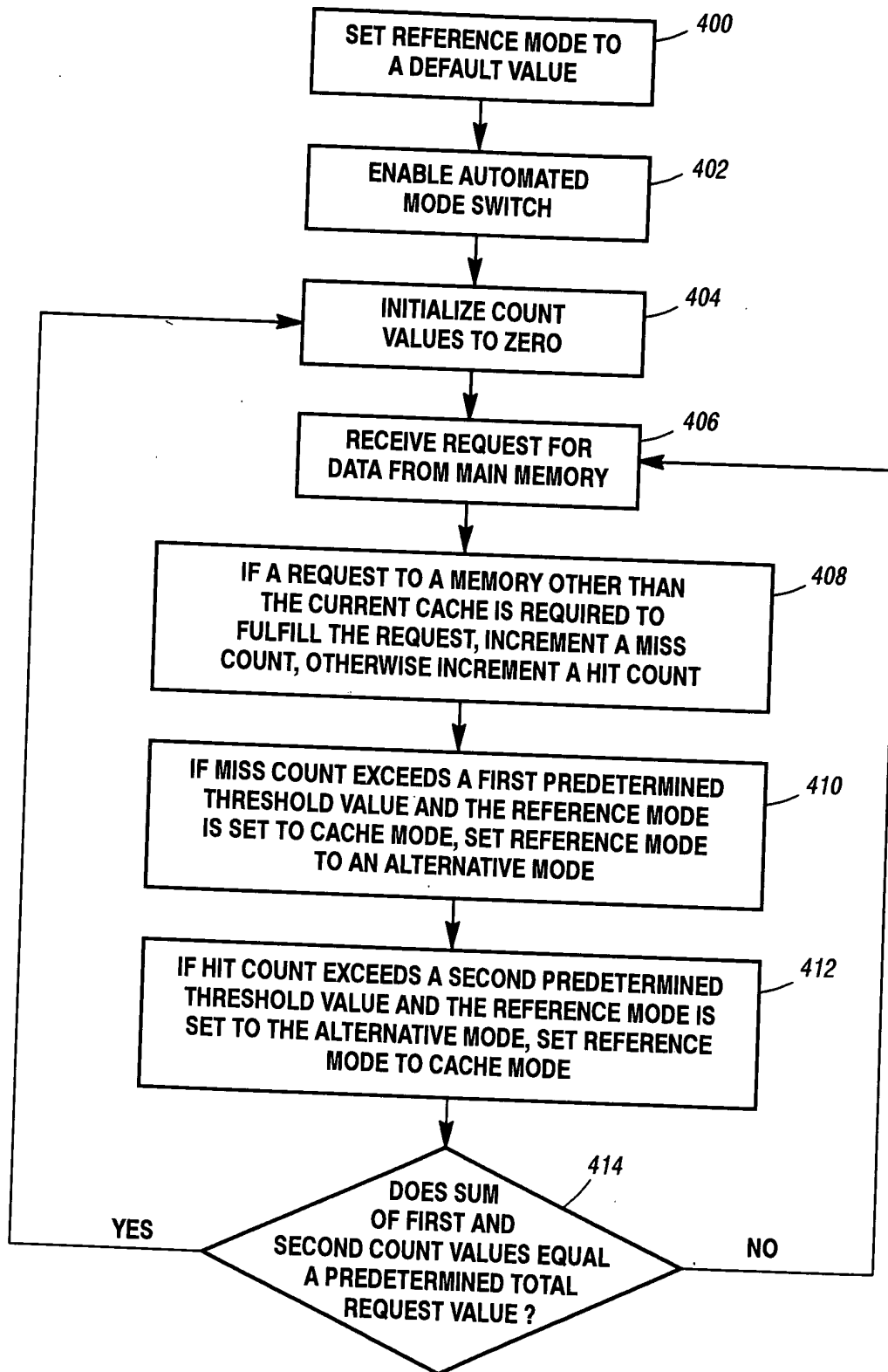


Figure 4

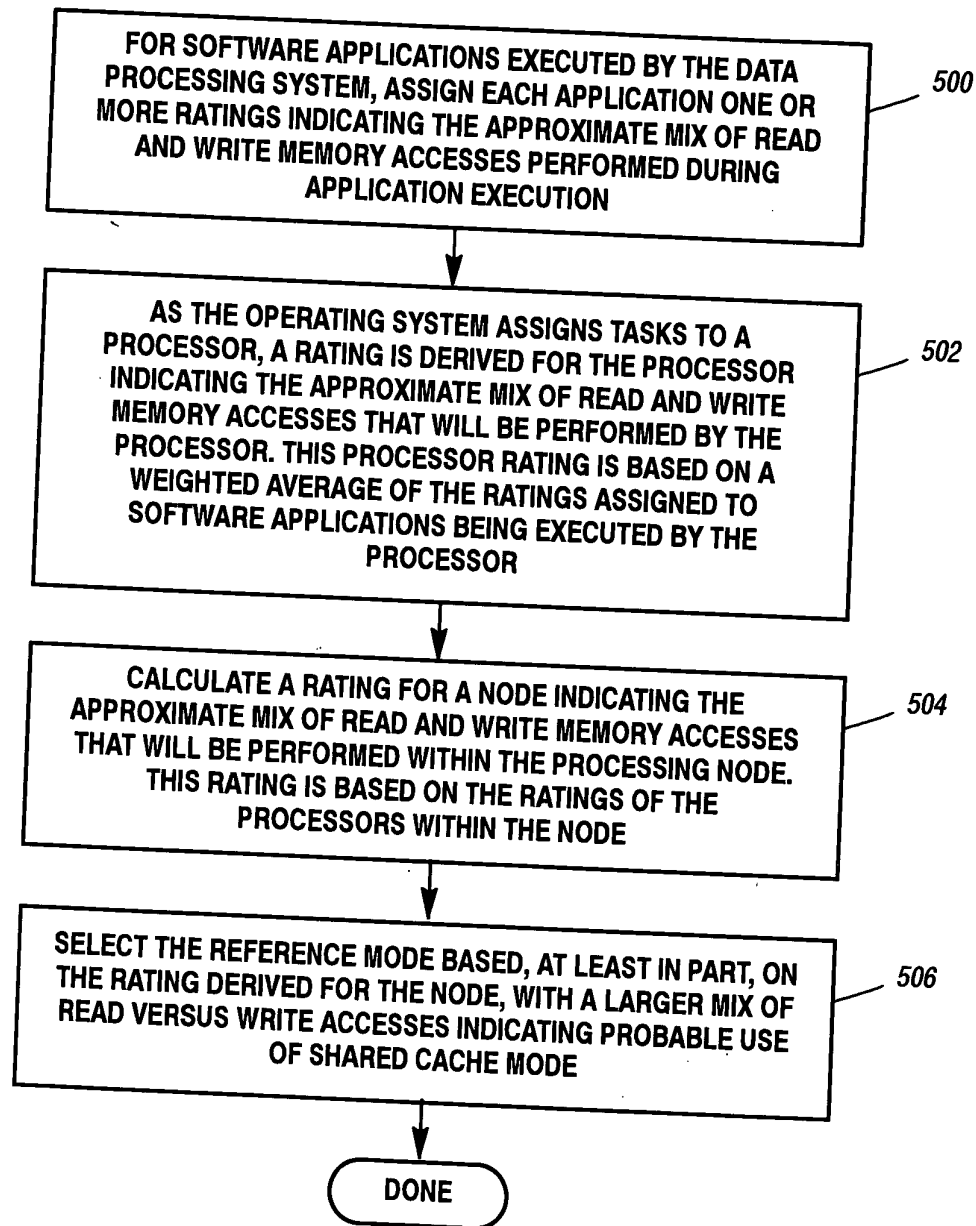


Figure 5